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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,518	06/02/2000	Michael R. Bruce	AMDA.455PA	5747

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EXAMINER
CHOI, SAM H

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 06/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/586,518	Applicant(s) BRUCE ET AL.	
	Examiner Sam H Choi	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6 and 7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not identify the citizenship of each inventor.

Drawings

2. Figure 1 is objected to because the elements included in it are not properly identified. Specifically, elements 100, 112, 114, 120, 124, and 150 are generic figures and are not identifiable. Correction is required.

Specification

3. The attempt to incorporate subject matter into this application by reference to the following applications:

"Method and Apparatus for Analyzing Functional Failures in Integrated Circuits" (Docket No. SD6542S93805)

"Data Processing Device Test Apparatus and Method Therefor" (Docket No. 184-P017US)

are improper because no application serial numbers are listed. Also, reference to the application:

"Thermally-induced Voltage Alteration (TIVA)" (Serial No. 09/034,546) is improper because no filing date is listed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,430,305 to Cole, Jr. et al.

Cole, Jr. et al. disclose a method for analyzing a semiconductor die having suspect circuitry that includes a multitude of circuit paths comprising: using a state-changing operation of the suspect circuitry to cause a failure due to the suspect circuitry (see column 9, lines 10-22; and column 13, lines 48-54); identifying one of the circuit paths that electrically changes in response to heat (see column 14, lines 15-60); and detecting that a particular circuit portion therein is resistive (see column 14, lines 50-67). Although Cole, Jr. et al. do not specifically state that the circuit portion is resistive, Cole, Jr. et al. disclose that the circuit portions, with a constant current source, change in voltage, requiring more electrical power (see column 14, lines 57-64). With power being equal to the voltage times the current, and the current being constant, the increase in power is due to the change in voltage, and more specifically, an increase in voltage. Since voltage is equal to the current times resistance, and, again, with the current being

constant, this would mean that the circuit portion has increased in resistance, becoming more resistive.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 3, 6-8, and 11-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cole, Jr. et al. in view of U.S. Patent No. 4,875,209 to Mathewes, Jr. et al.

Referring to claims 2, 3, 6-8, 11-16, and 18: as noted above, Cole, Jr. et al. disclose a method for analyzing a semiconductor die comprising: heating, with a laser (see Cole, Jr. et al., column 12, lines 3-21), at least a selected portion of state-changing circuitry in the semiconductor die to cause a failure due to suspect circuitry, the state-changing circuitry including a suspect signal line (see Cole, Jr. et al., column 13, lines 40-54); detecting, in response to the selected portion being heated, a state-changing transition (see Cole, Jr. et al., column 14, lines 34-67), which includes using a cross-sectional image of the operating circuitry and a map of signal paths, further comprising using the image and map to identify the location of the resistive signal path site (see Cole, Jr. et al., column 11, lines 56-61); using the detected state-changing transition, determining that the signal path site has a resistivity that changes (see Cole, Jr. et al.,

column 14, lines 50-67); electrically operating the die to cause the circuitry to change state in response to a controlled voltage supplied to the die (see Cole, Jr. et al., column 9, lines 10-22; and column 10, lines 34-44); using a scanning optical microscope (see Cole, Jr. et al., column 10, lines 54-65); and placing the die in a test arrangement adapted to electrically operate the die under selected operating conditions and to obtain a response from the die including state-changing transitions (see Cole, Jr. et al., column 10, lines 34-44). Although Cole, Jr. et al. do not specifically disclose heating at least a selected portion of state-changing circuitry including causing the suspect signal path site to expand, this is considered inherent to Cole, Jr. et al., because expansion of a signal path site would necessarily be present when applying heat to it. Cole, Jr. et al. do not disclose a method wherein the state-change transition is between a failed mode and a recovered mode in the signal path site. Mathewes, Jr. et al. disclose a method of testing an integrated circuit wherein the state-changing transition is between a failed mode and a recovered mode (see Mathewes, Jr. et al., column 9, lines 39-63). It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the method of Cole, Jr. et al., to include a step wherein the state-changing transition is between a failed mode and a recovered mode, as taught Mathewes, Jr. et al., because such a step would accurately verify fault detection by inserting known fault conditions and observing the results (see Mathewes, Jr. et al., column 2, lines 52-61).

Referring to claims 17 and 19-23: as noted above, Cole, Jr. et al. disclose a system for analyzing a semiconductor die comprising: a scanning optical microscope

(SOM) adapted to direct a laser and heat at least a selected portion of state-changing circuitry in the semiconductor die to cause a failure due to suspect circuitry, the state-changing circuitry including a suspect signal path site (see Cole, Jr. et al., column 9, lines 54-65; and Figure 1, element 12); wherein the SOM comprises a photodetector adapted to detect reflected light from the die as it is scanned with the laser and to provide a signal representing the detected light to the display (see Cole, Jr. et al., column 9, line 65 to column 10, line 6; and Figure 1, element 34); a position sensor adapted to provide the position of the laser upon the die (see Cole, Jr. et al., column 13, lines 40-62; and Figure 1, element 24); a detector adapted to detect, in response to the selected portion being heated, a state-changing transition in the signal path site (see Cole, Jr. et al., column 16, lines 52-68; and Figure 1, elements 26, 30, and 42); a display, which is communicatively coupled to the SOM and the detector (see Cole, Jr. et al., column 11, line 57 to column 12, line 2; and Figure 1, elements 12, 30, 26, and 30); including an image contrast amplifier, and wherein the detector includes an output adapted to supply a control signal to the image contrast amplifier in response to the transition (see Cole, Jr. et al., column 19, lines 16-40); adapted to use the detected state-changing transition and to display an image of the die to be used for determining that the signal path has a resistivity that changes (see Cole, Jr. et al., column 19, lines 5-40); and adapted to use the signal representing the detected light and the position sensor to display an image of the die, and wherein the contrast of the image of the resistive signal path is altered from that of a non-defective die (see Cole, Jr. et al., column 19, line 41 to column 20, line 2). Cole, Jr. et al. do not disclose a method

wherein the state-change transition is between a failed mode and a recovered mode in the signal path site. Mathewes, Jr. et al. disclose a method of testing an integrated circuit wherein the state-changing transition is between a failed mode and a recovered mode (see Mathewes, Jr. et al., column 9, lines 39-63). It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the method of Cole, Jr. et al., to include a step wherein the state-changing transition is between a failed mode and a recovered mode, as taught Mathewes, Jr. et al., because such a step would accurately verify fault detection by inserting known fault conditions and observing the results (see Mathewes, Jr. et al., column 2, lines 52-61).

8. Claims 4, 5, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cole, Jr. et al., in view of Mathewes Jr. et al., and further in view of U.S. Patent No. 5,557,559 to Rhodes.

As noted above, Cole Jr. et al., in combination with Mathewes Jr. et al., disclose a method for analyzing a semiconductor die. The combination, however, does not disclose a method further comprising electrically operating the die in a loop that causes the die to fail at a selected failure rate, and detecting a state-changing transition to include detecting that the failure rate has changed. Rhodes teaches a method of testing a semiconductor comprising electrically operating the die in a loop that causes the die to fail at a selected failure rate (see Rhodes, column 19, line 61 to column 20, line 3); and detecting a state-changing transition to include detecting that the failure rate has changed (see Rhodes, column 23, lines 1-28). It would have been obvious to one

having ordinary skill in the art, at the time the invention was made, to modify the method for analyzing a semiconductor die of Cole, Jr. et al., to include a step wherein the die is electrically operated in a loop to cause a selected failure rate, and wherein the detection of a state-changing transition includes detecting that the failure rate has changed, as taught by Rhodes, because such a step would reduce the time associated with semiconductor testing (see Rhodes, column 1, lines 47-64).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cole, Jr. et al., in view of Mathewes Jr. et al., and further in view of U.S. Patent No. 6,255,124 to Birdsley.

As noted above, Cole Jr. et al., in combination with Mathewes Jr. et al., disclose a method for analyzing a semiconductor die. The combination, however, does not disclose thinning the die prior to heating the die. Birdsley teaches a method of testing a semiconductor die, wherein the die is thinned before heating (see Birdsley, column 4, line 58 to column 5, line 18). It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the method for analyzing a semiconductor die of Cole, Jr. et al., to include a step wherein the die is thinned before heating, as taught by Birdsley, because such a step would reduce absorption losses of the laser (see Birdsley, column 2, lines 30-45).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cole, Jr. (U.S. Patent No. 6,078,183) discloses a semiconductor testing apparatus using a laser to thermally induce voltage changes in a semiconductor.

Nikawa (U.S. Patent No. 6,160,407) discloses a semiconductor testing apparatus using a laser to detect resistive defects in a semiconductor.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam H. Choi whose telephone number is (703) 305-1932. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff, can be reached at (703) 308-1677. The fax number for TC 2800 is (703) 308-7382. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (703) 308-1782.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging faxing responses of Office Actions directly into the Group at (703) 308-7382. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee, by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Sam H. Choi

28 May 2002

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